Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application.

1. (Previously Amended) A mixer circuit, comprising:

a signal input;

an RF transconductance circuit that is configured to convert an input differential signal received at said signal input to a differential current, said RF transconductance circuit having a pair of field effect transistors;

a LO switching circuit configured to switch said differential current between outputs of said mixer circuit at a rate determined by a differential LO signal; and

a variable current source that adds a DC current to said pair of field effect transistors in said RF transconductance circuit, said DC current adjusted so as to reduce flicker noise being generated inside the mixer circuit.

2. (Canceled)

3. (Canceled)

4. (Canceled)

5. (Original) The mixer circuit of claim 1, wherein said DC current bypasses said LO switching circuit.

6. (Previously Amended) A mixer circuit , comprising:

a signal input;

an RF transconductance circuit having a pair of field effect transistors (FETs) that are configured to convert an input differential signal received at said signal input to a differential current;

a LO switching circuit configured to switch said differential current between outputs of said mixer circuit at a rate determined by a differential LO signal;

a first variable current source configured to add a first DC current to a first FET of said pair of FETs; and

a second variable current source configured to add a second DC current to a second FET of said pair of FETs;

wherein said first DC current and said second DC current are determined so as to minimize flicker noise being generated inside of said mixer circuit.

7. (Canceled)

8. (Canceled)

9. (Original) The mixer circuit of claim 6, wherein said first DC current and said second DC current bypass said LO switching circuit.

10. (Original) The mixer circuit of claim 6, wherein said first DC current is added to a drain of said first FET in said pair of FETs, and said second DC current is added to a drain of said second FET in said pair of FETs.